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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,408	01/08/2002	Naoki Fukutomi	7426-082	9036

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EXAMINER	
BEREZNY, NEMA O	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/042,408	FUKUTOMI ET AL.	
	Examiner	Art Unit	
	Nema O. Berezny	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Amendment filed 3-2-05, which has been entered and considered. Claims 32-40 are currently pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 33-34 and 36-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Pennisi et al. (5,313,365). Pennisi discloses a substrate for mounting semiconductor devices thereon, having an insulating supporting member and plural sets of wirings, wherein said wirings form a predetermined wiring pattern including a wire bonding terminal (Fig.1 el.12) and an external connection terminal (Fig.2 el.27); and said external connection terminal is provided only inside of said wire bonding terminal (Fig.1) **[claim 33]**; comprising a plurality of said wiring patterns comprised of a plurality of said wirings arranged in rows and columns (Fig.2) **[claim 34]**; wherein said external connection terminal is one of a plurality of external connection terminals, exposed on a surface of said insulating supporting member, on an opposite side to which said semiconductor device is mounted, and said external connection terminals are arranged

in a grid pattern at positions corresponding to a semiconductor device mounting region and a semiconductor package region of said substrate (Figs.1-2) **[claim 36]**; and a semiconductor package produced by a method comprising the steps of: mounting a semiconductor device on each of said plural semiconductor device mounting regions of the substrate for mounting the semiconductor device thereon according to claim 33 by employing a die-bonding material, electrically connecting the semiconductor device with the wire-bonding terminals by wire-bonding, sealing said semiconductor package region including said semiconductor device with a sealing resin connected in one-piece; forming solder bumps on said external connection terminals; and cutting said substrate for mounting the semiconductor device thereon and said sealing resin in one operation to be separated into the individual semiconductor package (Figs.1,2) **[claim 37]**.

Based upon the rejection of claim 33 above, Pennisi also discloses wherein said external connection terminal is one of a plurality of external connection terminals, exposed on a surface of said insulating supporting member, on an opposite side to which said semiconductor device is mounted, and wherein all of said plurality of external connection terminals are located only inside of said wire bonding terminal (Fig.1) **[claim 38]**; wherein said wire bonding terminal is one of a plurality of wire bonding terminals of said substrate, and wherein said plurality of external connection terminals are positioned only within the plurality of the wire bonding terminals (Fig.1) **[claim 39]**; and wherein said wire bonding terminal is one of a plurality of wire bonding terminals of said substrate, and wherein said at least one external connection terminal is positioned only inside of the plurality of wire bonding terminals (Fig.1) **[claim 40]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pennisi et al. (5,313,365) in view of Dougherty, Jr. et al. (4,602,271). Pennisi discloses a substrate for mounting semiconductor devices thereon having an insulating supporting member and plural sets of wirings, and further comprising: a semiconductor device mounting region (Figs.1-2 el.11) and a resin-sealing semiconductor package region (el.15) outside of said semiconductor device mounting region, wherein said plural sets of wirings comprise a predetermined wiring pattern including wire-bonding terminals (el.13) and external connection terminals (el.27), wherein said wire bonding terminals are provided in said semiconductor package region and said external connection terminals are provided only within said semiconductor device mounting region (Figs.1-2). However, Pennisi does not disclose wherein said substrate includes a plurality of said semiconductor device mounting regions, and wherein said plurality of said semiconductor device mounting regions respectively have blocks of said wirings, each having a same pattern. Pennisi would look to one such as Dougherty for efficient mass fabrication because Dougherty discloses wherein said substrate includes a plurality of said semiconductor device mounting regions, and wherein said plurality of said

semiconductor device mounting regions respectively have blocks of said wirings, each having a same pattern (Abstract). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the plurality of mounting regions of Dougherty with the substrate of Pennisi since a single substrate can be used to mount several chips, thereby decreasing fabricating steps and time (col.3 lines 48-53).

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pennisi as applied to claim 33 above, and further in view of Katsuhiko (JP 59208756). Pennisi does not disclose a nickel and/or gold plate layer on said wire-bonding terminal. However, Pennisi would look to one such as Katsuhiko for migration and oxidation resistance because Katsuhiko discloses wherein said wire-bonding terminal comprises a nickel layer and a gold plate layer on its surface (Abstract). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the nickel and gold layers of Katsuhiko with the substrate of Pennisi; nickel acts as a migration resistant layer, and gold provides oxidation resistance (inherent properties of nickel and gold).

Response to Arguments

Applicant's arguments filed 3-2-05, regarding claims 32-37 have been fully considered but they are not persuasive. All of Applicant's arguments are based upon the contention that Pennisi does not disclose external connection terminals, or at least

one external connection terminal, or a plurality of external connection terminals being located within the semiconductor device mounting region, or located inside of the wire bonding terminals on the opposite side of the substrate. Examiner disagrees. The claim element of "at least one external connection terminal" is satisfied if one external connection is disclosed by Pennisi. The claim elements of "external connection terminals" and "a plurality of external connection terminals" are satisfied if two external connections are disclosed by Pennisi. Fig.1 of Pennisi discloses a side view of a device mounted on the top surface of a substrate, having wire bonding terminals on the substrate top surface and external connections located on the substrate bottom surface, and also discloses encapsulation of the device and wire bonding terminals. For the sake of argument, Examiner has selected the middle two bottom external connections to satisfy the claim elements of "at least one," "external connections," and "a plurality of" external connections. These two inside external connections satisfy the claim elements of being located within the device mounting region, and being located inside of the wire bonding terminals. Therefore, Pennisi properly discloses the claim elements of previously rejected claims 32-37 as cited in the prior and instant Office Actions, as well as new claims 38-40.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O. Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan H. Nguyen

NB

Tuan H. Nguyen
Primary Exam[illegible]